[Total No. of Questions - 9] [Total No. of Printed Pages - 3] (2125)

15315

B. Tech 7th Semester Examination

Digital System Design Using HDL (NS)

EC-412

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all, any one question from section A, B, C and D and all parts of section E.

SECTION - A

1. (a) Write the code for a 2-bit full adder using

   (i) Data flow method.

   (ii) Structural method. (10)

   (b) Write the test bench to verify a 4-bit carry looks ahead adder (10)

2. (a) Declare a two dimensional array. Write a process to read from the array and to write into the array. (5)

   (b) When do we use a function? Give an example. (5)

   (c) Are loops Synthesizable? Give an example and draw the synthesized hardware. (5)

   (d) How can a code be customized using generics? Give an example. (5)

[P.T.O.]

SECTION - B

3 (a) Write the code and Draw the Hardware equivalent for both flip-flops.

   (i) Synchronous reset D-FF with positive edge triggered clock.

   (ii) Asynchronous reset D-FF with negative edge triggered clock. (10)

   (b) Write the code to implement and test a circular buffer of depth 256 bytes. (10)

4. (a) Implement a barrel shifter for 4 bit data. Write a test bench to verify the same. (10)

   (b) Design a MOD 13 counter using negative edges triggered D flip flop. Write the code for the same. (10)

SECTION - C

5. (a) Write short notes on clocks and the problems associated in routing them. (10)

   (b) Implement a synchronous FIFO of depth 64 bytes. (10)

6. (a) How is synchronization done across clock domains? Explain with an example. (5)

   (b) Why is gated clock not preferred? When do you use a gated clock in spite of its disadvantages? (5)

   (c) Describe any two memory implementations with their respective VHDL code. (10)

SECTION - D

7. Draw a CLB of a Xilinx FPGA and explain its components. (20)

8. Write the code to implement and test a circular buffer of depth 256 bytes. (20)

SECTION - E

9. (a) Write the code for a 4×2 priority encoder.

(b) List the types of delay available in VHDL with examples.

(c) Write two statements for writing values onto a file and read from the same file.

(d) Define synthesis. Name some non-synthesizable statements in VHDL.

(e) What is a clock buffer? Where it is used?

(f) Draw a 4-cell DRAM.

(g) When and how a design partition is performed?

(h) List a few post synthesis parameter to be verified.

(i) Draw a slice in a XLINX FPGA.

(j) Implement a function $F=\Sigma(1,7)$ in a 3 input LUT.

(2×10=20)